Terms used **executable instructions constraint** Found **778** of **164,603**

Sort results by: relevance
Display results: expanded form
Save results to a Binder
Search Tips
Open results in a new window

Try an Advanced Search
Try this search in The ACM Guide

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next
Best 200 shown Relevance scale

1 Limits of control flow on parallelism
Monica S. Lam, Robert P. Wilson
April 1992 **ACM SIGARCH Computer Architecture News , Proceedings of the 19th annual international symposium on Computer architecture**, Volume 20 Issue 2
Full text available: pdf(1.30 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper discusses three techniques useful in relaxing the constraints imposed by control flow on parallelism: control dependence analysis, executing multiple flows of control simultaneously, and speculative execution. We evaluate these techniques by using trace simulations to find the limits of parallelism for machines that employ different combinations of these techniques. We have three major results. First, local regions of code have limited parallelism, and control dependence analysis ...

2 Is SC + ILP = RC?
Chris Gniady, Babak Falsafi, T. N. Vijaykumar
May 1999 **ACM SIGARCH Computer Architecture News , Proceedings of the 26th annual international symposium on Computer architecture**, Volume 27 Issue 2
Full text available: pdf(94.82 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Sequential consistency (SC) is the simplest programming interface for shared-memory systems but imposes program order among all memory operations, possibly precluding high performance implementations. Release consistency (RC), however, enables the highest performance implementations but puts the burden on the programmer to specify which memory operations need to be atomic and in program order. This paper shows, for the first time, that SC implementations can perform as well as RC implementations ...

3 Instruction Scheduling for Dynamic Hardware Configurations
Elena Moscu Panainte, Koen Bertels, Stamatis Vassiliadis
March 2005 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 1**
Full text available: pdf(165.23 KB) Additional Information: full citation, abstract

Although the huge reconfiguration latency of the available FPGA platforms is a well-known shortcoming of the current FCCMs, little research in instruction scheduling has been undertaken to eliminate or diminish its negative influence on performance. In this paper, we introduce an instruction scheduling algorithm that minimizes the number of executed

Freeform Search

Database: US Pre-Grant Publication Full-Text Database; **US Patents Full-Text Database**; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Term: L71 and RSVP

Display: 30 **Documents in Display Format:** CIT **Starting with Number** 1

Generate: ○ **Hit List** ◉ **Hit Count** ○ **Side by Side** ○ **Image**

Search | Clear | Interrupt

Search History

DATE: Monday, October 17, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT; PLUR=YES; OP=ADJ			
L73	L71 and RSVP	9	L73
L72	L71 and RESV	1	L72
L71	L70 and path near determination	10	L71
L70	constraint and LSR	382	L70
L69	L66 and instruction	1	L69
L68	L66 and determination	0	L68
L67	L66 and determination and path	0	L67
L66	L64 and LSP	5	L66
L65	L64 and LSR	0	L65
L64	constraint near RSVP	6	L64
L63	L61 and router	1	L63
L62	L61 and LSR	0	L62
L61	constraint near executable	6	L61
L60	constraint near executable and path and determination	0	L60
L59	L58 and router	0	L59
L58	L56 and path and determination	17	L58

L57	L56 and LSR	0	L57
L56	execute near constraints	52	L56
L55	L54 and LSR	1	L55
L54	L53 and forwarding near message	8	L54
L53	L52 and RSVP	113	L53
L52	executable adj instruction	26362	L52
L51	path near determination near policy	0	L51
L50	path near determination near constraint	0	L50
L49	L48 and loose	7	L49
L48	L47 and path and determination	53	L48
L47	L46 and LSR	89	L47
L46	constraints and message and RSVP	452	L46
L45	RSVP near contraints	0	L45
L44	l41 and constraint-based	0	L44
L43	L41 and RSVP	0	L43
L42	L41 and LSR	0	L42
L41	L40 and path	61	L41
L40	L38 and determination	98	L40
L39	L38 and path near determination	0	L39
L38	constraint near instructions	213	L38
L37	L36 and instruction	1	L37
L36	L35 and path near determination	4	L36
L35	signaling near message and constraint	824	L35
L34	L33 and path and executable	4	L34
L33	determination near constraint and instructions	53	L33
L32	constaint near executable near instruction	0	L32
L31	constaint near executable near function	0	L31
L30	L28 and executable	8	L30
L29	L28 and execute	6	L29
L28	L27 and instructions	8	L28
L27	L26 and message	8	L27
L26	L25 and path and determination	12	L26
L25	L22 and LSR	32	L25
L24	L23 and LSR	2	L24
L23	L22 and path near determination	31	L23
L22	executable near instruction and constraint	6608	L22
L21	L19 and instructions and executable	2	L21
L20	L19 and instructions and execute	3	L20
L19	L18 and LSR	9	L19
L18	L17 and constraints	36	L18
L17	PATH near RSVP	149	L17

L16	PATH RSVP and message and LSR	1	L16
L15	l14 and PATH near RSVP	0	L15
L14	L13 and constraint	10	L14
L13	L12 and path near determination	10	L13
L12	L11 and LSRs	382	L12
L11	constraint and LSR	382	L11
L10	L9 and LSP	0	L10
L9	L8 and determination near constraint	19	L9
L8	message and path near determination and constraints	164	L8
L7	L6 and path near determination	3	L7
L6	constraint near processing	1150	L6
L5	L4 and message	7	L5
L4	L3 and constraint-based	10	L4
L3	constraint and path near determination	309	L3
L2	constraint-based near path near determination	0	L2
L1	message near carring and path near determination	0	L1

END OF SEARCH HISTORY